ABSTRACT OF THE DISCLOSURE

A multi-stage bit stream multiplexer that divides multiplexing functions between two or more integrated circuits. The first integrated circuit receives 16 bit streams to produce 4 output bits streams with a nominal data rate of 10 GBPS. A second integrated circuit multiplexes the 4 streams and to a bit stream with a data rate of 40 GBPS. The first IC is made in a standard CMOS process while the second IC is made using processes that support higher switching rates. The first IC produces a source-centered double data rate forward transmit clock from a reference clock selectable from either a crystal oscillator, a voltage controlled oscillator using a loop clock from the receive side of the bit stream multiplexer or a reverse clock generated by the second IC. The reverse clock can be selected as the source of the reference either by default, or in response to a specific condition.